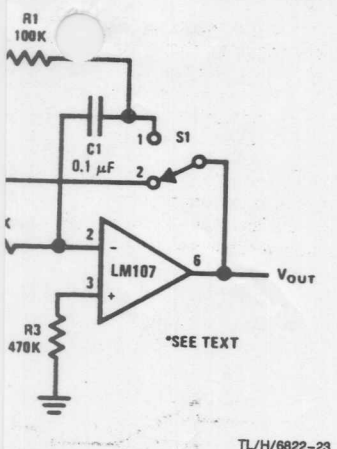


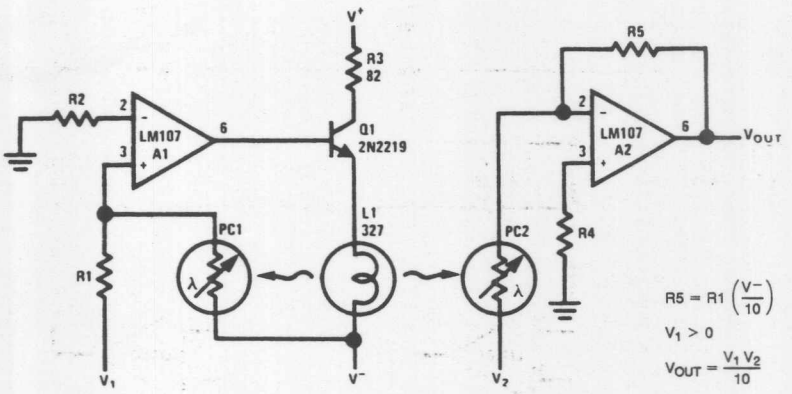
TL/H/6822–23

1. Reset Stabilized Amplifier

seful in eliminating errors due to offset
rent. The output of this circuit is a pulse
equal to V_{IN}. Operation may be under-
g the two conditions corresponding to
/hen S_1 is in position 2, the amplifier is
ity gain connection and the voltage at
ual to the sum of the input offset volt-
ross R2 due to input bias current. The
ing input will be equal to input offset
1 will charge to the sum of input offset
ugh R1. When C1 is charged, no cur-
e source resistance and R1 so there is
resistance. S_1 is then changed to posi-
stored on C1 is inserted between the
nput of the amplifier and the output of
by V maintain the amplifier input
oltage. output then changes from
$V_{IN} + I_{bias}R2$) as S_1 is changed from
1. Amplifier bias current is supplied
utput of the amplifier or from C2 when
position 1 respectively. R3 serves to
e amplifier output if the amplifier must
range or if it is desired to DC couple

ge of this connection is that input re-
infinity as the capacitor C1 ap-
liminating errors due to loading of the
e time spent in position 2 should be
he charging time of C1 for maximum

st be compensated for unity gain op-
necessary to overcompensate be-
ft across R2 due to C1 and the ampli-
ce this connection is usually used at
ds, slew rate is not normally a practi-
overcompensation does not reduce



TL/H/6822–24

FIGURE 22. Analog Multiplier

THE ANALOG MULTIPLIER

A simple embodiment of the analog multiplier is shown in *Figure 22*. This circuit circumvents many of the problems associated with the log-antilog circuit and provides three quadrant analog multiplication which is relatively temperature insensitive and which is not subject to the bias current errors which plague most multipliers.

Circuit operation may be understood by considering A2 as a controlled gain amplifier, amplifying V_2, whose gain is dependent on the ratio of the resistance of PC2 to R5 and by considering A1 as a control amplifier which establishes the resistance of PC2 as a function of V_1. In this way it is seen that V_{OUT} is a function of both V_1 and V_2.

A1, the control amplifier, provides drive for the lamp, L1. When an input voltage, V_1, is present, L1 is driven by A1 until the current to the summing junction from the negative supply through PC1 is equal to the current to the summing junction from V_1 through R1. Since the negative supply voltage is fixed, this forces the resistance of PC1 to a value proportional to R1 and to the ratio of V_1 to V^-. L1 also illuminates PC2 and, if the photoconductors are matched, causes PC2 to have a resistance equal to PC1.

A2, the controlled gain amplifier, acts as an inverting amplifier whose gain is equal to the ratio of the resistance of PC2 to R5. If R5 is chosen equal to the product of R1 and V^-, then V_{OUT} becomes simply the product of V_1 and V_2. R5 may be scaled in powers of ten to provide any required output scale factor.

PC1 and PC2 should be matched for best tracking over temperature since the T.C. of resistance is related to resistance match for cells of the same geometry. Small mismatches may be compensated by varying the value of R5 as a scale factor adjustment. The photoconductive cells should receive equal illumination from L1, a convenient method is to mount the cells in holes in an aluminum block and to mount the lamp midway between them. This mounting method provides controlled spacing and also provides a thermal bridge between the two cells to reduce differences in cell temperature. This technique may be extended to the use of FET's or other devices to meet special resistance or environment requirements.

The circuit as shown gives an inverting output whose magnitude is equal to one-tenth the product of the two analog inputs. Input V_1 is restricted to positive values, but V_2 may assume both positive and negative values. This circuit is restricted to low frequency operation by the lamp time constant.

R2 and R4 are chosen to minimize errors due to input offset current as outlined in the section describing the photocell amplifier. R3 is included to reduce in-rush current when first turning on the lamp, L1.

THE FULL-WAVE RECTIFIER AND AVERAGING FILTER

The circuit shown in *Figure 23* is the heart of an average reading, rms calibrated AC voltmeter. As shown, it is a rectifier and averaging filter. Deletion of C2 removes the averaging function and provides a precision full-wave rectifier, and deletion of C1 provides an absolute value generator.

Circuit operation may be understood by following the signal path for negative and then for positive inputs. For negative signals, the output of amplifier A1 is clamped to +0.7V by D1 and disconnected from the summing point of A2 by D2. A2 then functions as a simple unity-gain inverter with input resistor, R1, and feedback resistor, R2, giving a positive going output.

For positive inputs, A1 operates as a normal amplifier connected to the A2 summing point through resistor, R5. Amplifier A1 then acts as a simple unity-gain inverter with input

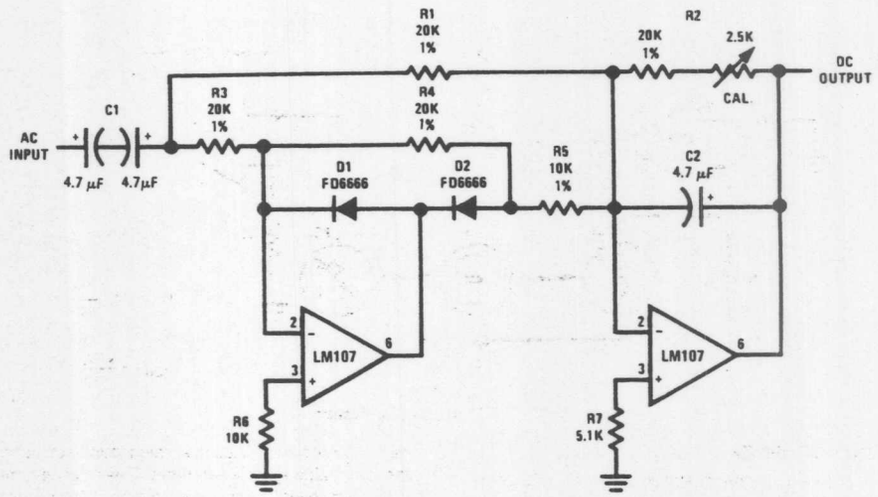


FIGURE 23. Full-Wave Rectifier and Averaging Filter

resistor, R3, and feedback resistor, R5. A1 gain accuracy is not affected by D2 since it is inside the feedback loop. Positive current enters the A2 summing point through resistor, R1, and negative current is drawn from the A2 summing point through resistor, R5. Since the voltages across R1 and R5 are equal and opposite, and R5 is one-half the value of R1, the net input current at the A2 summing point is equal to and opposite from the current through R1 and amplifier A2 operates as a summing inverter with unity gain, again giving a positive output.

The circuit becomes an averaging filter when C2 is connected across R2. Operation of A2 then is similar to the Simple Low Pass Filter previously described. The time constant R2C2 should be chosen to be much larger than the maximum period of the input voltage which is to be averaged.

Capacitor C1 may be deleted if the circuit is to be used as an absolute value generator. When this is done, the circuit output will be the positive absolute value of the input voltage.

The amplifiers chosen must be compensated for unity-gain operation and R6 and R7 must be chosen to minimize output errors due to input offset current.

SINE WAVE OSCILLATOR

An amplitude-stabilized sine-wave oscillator is shown in *Figure 24*. This circuit provides high purity sine-wave output down to low frequencies with minimum circuit complexity. An important advantage of this circuit is that the traditional tungsten filament lamp amplitude regulator is eliminated along with its time constant and linearity problems.

In addition, the reliability problems associated with a lamp are eliminated.

The Wien Bridge oscillator is widely used and takes advantage of the fact that the phase of the voltage across the parallel branch of a series and a parallel RC network connected in series, is the same as the phase of the applied voltage across the two networks at one particular frequency and that the phase lags with increasing frequency and leads with decreasing frequency. When this network—the Wien Bridge—is used as a positive feedback element around an amplifier, oscillation occurs at the frequency at which the phase shift is zero. Additional negative feedback is provided to set loop gain to unity at the oscillation frequency. To stabilize the frequency of oscillation, and to reduce harmonic distortion.

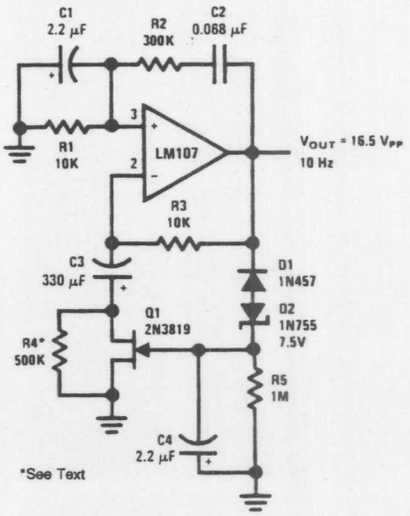


FIGURE 24. Wien Bridge Sine Wave Oscillator

The circuit presented here differs from the classic usage only in the form of the negative feedback stabilization scheme. Circuit operation is as follows: negative peaks in excess of −8.25V cause D1 and D2 to conduct, charging